

# LVDS RX I/O cell

## Product description

The RX cell is a high-speed and low-power LVDS receiver IO cell powered at 2.5V/1.1V or 1.8V/1.1V, designed on the TSMC 40 LP technology.

## Main characteristics

- TSMC 40 LP
- 2.5V/1.1V IO/Core transistors
- Fully compliant with TIA/EIA-644-A-2001

## Deliverables

- GDS II layouts
- LEF abstracts
- CDL netlists
- Liberty timings
- Verilog description
- A full datasheet
- An integration note

## Status

- Silicon proven

## Applications

- Multi-purpose reconfigurable IO
- Point-to-point, point-to-multipoint or bus-based IC high-speed data communications
- Intra-package (e.g. MCM or SIP) inter-die high-speed data communications
- Backplane high-speed data communications
- High-speed serial communications (HDMI, SATA, PCIeX, etc.)
- Communication to LCD/OLED screens
- Video sensor digital data interface

## Main features

- Standard-compliant to TIA/EIA-644-A-2001
- Built-in, low parasitic ESD protection
- Easily integrates with TSMC I/O library cells
- All-in-ring® topology, so no core silicon area is used by LVDS
- The same cells operate with 2.5V/1.1V or 1.8V/1.1V power supplies
- Standby/power down mode
- Internal bias voltage generation and bias current distribution circuitry
- Selectable on-chip termination resistor, with optional user tuning
- Digital loopback functions to ease ATE testing
- Up to 2 Gbps data rate



## Further information

For further information about this product and other products of the nSIO\_TS40LP\_2V5\_1V1 transmit / receive / combo LVDS IO library, development roadmap, availability and licensing terms, please e-mail to [sales@nsilition.com](mailto:sales@nsilition.com).

## Delivery and support

These LVDS IOs are available as hard macro-cells for reuse in any design based on the TSMC 40 LP with 2.5V IO transistors CMOS process. No extra IP license from any third party will be needed for the cells or the cell library.

In addition, full support service is available on request. Support can include close integration follow-up by our design team or custom-made cells or features. nSilitation may provide support to the Customer for qualifying the maximum clocking frequency corresponding to the selected chip package and the PCB LVDS track length and impedance. IBIS models for digital outputs can be provided upon request.

## Porting to another process

The nSIO\_TS40LP\_2V5\_1V1 transmit/receive LVDS IO library is silicon proven in the TSMC 40 LP 2.5V/1.1V CMOS process. It can be easily ported to another foundry and/or another similar CMOS process node upon request. Please contact us for details and availability.

## About nSilitation

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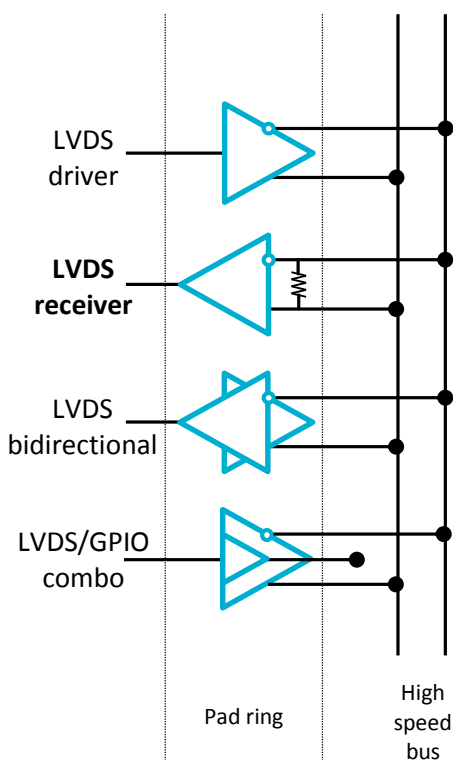
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*Available LVDS cells in nSIO\_TS40LP\_2V5\_1V1 IP library*



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