

# LVDS TX I/O cell

## Product description

The TX cell is a high-speed and low-power LVDS transmitter IO cell powered at 2.5V/1.2V or 1.8V/1.2V, designed on the TSMC 65 GP technology.

### Main characteristics

- TSMC 65 GP
- 2.5V/1.2V IO/Core transistors
- Fully compliant with TIA/EIA-644-A-2001

### Deliverables

- GDS II layouts
- LEF abstracts
- CDL netlists
- Liberty timings
- Verilog description
- A full datasheet
- An integration note

### Status

- Silicon proven

- Applications
- Multi-purpose reconfigurable IO
- Point-to-point, point-to-multipoint or bus-based IC high-speed data communications
- Intra-package (e.g. MCM or SIP) inter-die high-speed data communications
- Backplane high-speed data communications
- High-speed serial communications (HDMI, SATA, PCIeX, etc.)
- Communication to LCD/OLED screens
- Video sensor digital data interface

## Main features

- Standard-compliant to TIA/EIA-644-A-2001
- Built-in, low parasitic ESD protection
- Easily integrates with TSMC I/O library cells
- All-in-ring® topology, so no core silicon area is used by LVDS
- The same cells operate with 2.5V/1.2V or 1.8V/1.2V power supplies
- Adjustable output common mode voltage (LVDS or SubLVDS mode)
- Adjustable driving current for buses with single or double termination
- Standby/power down mode
- Internal bias voltage generation and bias current distribution circuitry
- Selectable on-chip termination resistor, with optional user tuning
- Digital loopback functions to ease ATE testing
- Up to 2 Gbps data rate



## Further information

For further information about this product and other products of the nSIO\_TS65LP\_2V5\_1V2 transmit / receive / combo LVDS IO library, development roadmap, availability and licensing terms, please e-mail to [sales@nsilition.com](mailto:sales@nsilition.com).

## Delivery and support

These LVDS IOs are available as hard macro-cells for reuse in any design based on the TSMC 65 GP with 2.5V IO transistors CMOS process. No extra IP license from any third party will be needed for the cells or the cell library.

In addition, full support service is available on request. Support can include close integration follow-up by our design team or custom-made cells or features. nSilitation may provide support to the Customer for qualifying the maximum clocking frequency corresponding to the selected chip package and the PCB LVDS track length and impedance. IBIS models for digital outputs can be provided upon request.

## Porting to another process

The nSIO\_TS65LP\_2V5\_1V2 transmit/receive LVDS IO library is silicon proven in the TSMC 65 GP 2.5V/1.2V CMOS process. It can be easily ported to another foundry and/or another similar CMOS process node upon request. Please contact us for details and availability.

## About nSilitation

nSilitation is a leading analog and mixed-signal semiconductor IP provider. nSilitation specializes in the development of high quality analog and mixed-signal high performance semiconductor IPs. With reference designs available for 10b to 14b A/D and D/A converters, high-speed IO circuits, PFM and PWM high efficiency DC/DC integrated converters and high precision bandgap references; nSilitation enables the highest value analog and mixed-signal functionalities at the lowest risk.

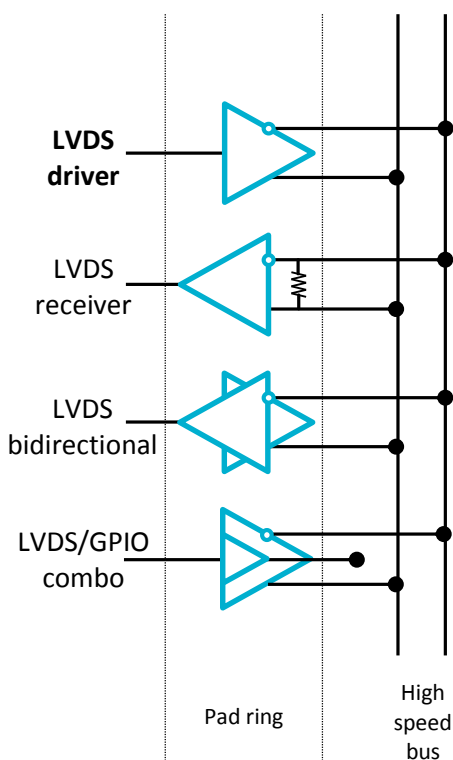
The "IP design" service of nSilitation offers top-class quality, customization and support dedicated to your needs and your specifications.

## Disclaimer

The information provided by nSilitation has been verified and is believed to be accurate. nSilitation and all its right holders reserve the right to make changes to the information contained herein without notice. They reserve also the right to make changes to the product without notification. No liability shall be incurred as a result of the use or application of the information provided in this data sheet and/or the use of the corresponding product in any case.

Copyright © 2014 nSilitation sprl  
31, bd Dolez, 7000 Mons (Belgium)  
VAT: BE 885821519

*Support can include close integration follow-up by our design team or custom-made cells or features*



*Available LVDS cells in nSIO\_TS65LP\_2V5\_1V2 IP library*



**nSilitation**  
Smaller, Smarter, Stronger